What is claimed is:

1. A method of synchronizing one or more devices on a first bus with one or more devices on a second bus, the method comprising:

acquiring timing information from the first bus and the second bus;

determining a timing offset between the first bus and the second bus; and,

broadcasting the timing offset to the one or more devices on the second bus so that the one or more devices on the second bus can adjust their timing to be synchronized with the one or more devices on the first bus.

2. A method according to claim 1 wherein acquiring timing information from the first bus and the second bus comprises:

taking a first time measurement for the first bus;

taking a time measurement for the second bus; and,

taking a second time measurement for the first bus;

and wherein determining the timing offset comprises:

calculating an average of the first and second time measurements for the first bus; and

subtracting the time measurement for the second bus from the average.

3. A method according to claim 1 comprising calculating a drift rate of the timing offset and broadcasting the drift rate along with the timing offset.

4. A method according to claim 3 wherein calculating the drift rate comprises calculating a first order time derivative.

5. A method according to claim 3 wherein calculating the drift rate comprises calculating a second order time derivative.

6. A method according to claim 1 wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus.

7. A method according to claim 6 wherein the one or more devices on the second bus adjust their timing by determining timing information of the first bus by applying the timing offset to the timing information of the second bus.

8. A method according to claim 1 wherein the one or more devices on the second bus adjust their timing by adjustably controlling a delay to alter a length of an operational cycle.

9. A method according to claim 1 wherein the one or more devices on the second bus comprise cameras and the cameras adjust their timing by selectively reading an adjustable amount of extra data for each frame.

10. A method according to claim 1 wherein the first and second buses comprise serial buses.

11. A method according to claim 1 wherein the first and second buses comprise USB buses.

12. A method according to claim 1 wherein the first and second buses comprise buses compliant with electronics standard IEEE 1394.

13. A method according to claim 1 wherein the first and second buses comprise different types of buses.

14. A method according to claim 1 comprising respectively associating first and second clocks with the first and second buses for generating timing information for the first and second buses.

15. A method according to claim 14 comprising automatically broadcasting timing information on the first and second buses

16. A method according to claim 14 wherein the method is carried out on a data processor comprising first and second interfaces coupled to the first and second buses, respectively, and wherein acquiring timing information from the first bus and the second bus comprises querying the first and second interfaces for the timing information.

17. A method according to claim 14 wherein the method is carried out on a synchronization unit coupled between the first and second buses, and wherein acquiring timing information from the first bus and the second bus comprises receiving timing information from the first and second clocks.

18. A method of synchronizing one or more devices on a first bus with one or more devices on a second bus, the method comprising:

(a) taking a first time measurement for the first bus;

(b) taking a time measurement for the second bus;

(c) taking a second time measurement for the first bus;

(d) calculating an average of the first and second time measurements for the first bus;

(e) subtracting the time measurement for the second bus from the average to determine a timing offset between the first bus and the second bus;

(f) storing the timing offset;

(g) if at least two timing offsets have been stored, calculating a drift rate based at least in part on a difference between two of the stored offsets and a time elapsed between when the two stored offsets were determined, otherwise setting the drift rate to zero;

(h) broadcasting the timing offset and the drift rate onto the second bus so that the one or more devices on the second bus can adjust their timing to be synchronized with the one or more devices on the first bus; and,

(i) repeating steps (a) through (h).

19. A method of synchronizing one or more devices on a first bus with one or more devices on a second bus, the method comprising:

providing a separate master bus on which a global time is broadcast by a master clock;

acquiring timing information from the first bus and the second bus;

determining a first timing offset between the first bus and the separate master bus;

determining a second timing offset between the second bus and the separate master bus; and,

broadcasting the first timing offset to the one or more devices on the first bus and the second timing offset to the one or more devices on the second bus so that the one or more devices on the first bus and the one or more devices on the second bus all begin their respective operational cycles at the same global time.

20. A method according to claim 19 wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on the global time.

21. A method according to claim 20 wherein the one or more devices on the first and second buses each adjust their timing by determining the global time by applying the timing offset to the timing information of the first and second buses, respectively.

22. An apparatus for synchronizing one or more devices on a first bus with one or more devices on a second bus, the apparatus comprising:

a first interface coupled to the first bus;

a second interface coupled to the second bus;

a processing element coupled to the first and second interfaces to receive timing information for the first and second buses; and,

a program memory coupled to the processing element, the program memory containing software instructions programmed to cause processing element to calculate a timing offset between the first bus and the second bus and broadcast the timing offset to the one or more devices on the second bus by means of the second interface.

23. An apparatus according to claim 22 wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus.

24. An apparatus according to claim 23 wherein the one or more devices on the second bus are configured to adjust their timing by determining timing information of the first bus by applying the timing offset to the timing information of the second bus.

25. An apparatus according to claim 22 wherein a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses.

26. An apparatus according to claim 22 wherein the first and second interfaces, the processing element and the program memory are all

located within a data processor configured to process data received from the one or more devices on the first bus and the one or more devices on the second bus.

27. An apparatus according to claim 22 wherein the first interface, the processing element and the program memory are all located within a first data processor configured to process data received from the one or more devices on the first bus and second interface is located within a second data processor configured to process data received from the one or more devices on the second bus, and wherein the first and second data processors are connected by a network connection.

28. An apparatus according to claim 22 wherein the first and second interfaces, the processing element and the program memory are all located within a synchronization unit coupled between the first and second buses.

29. An apparatus according to claim 22 wherein the one or more devices on the first bus comprise a first plurality of cameras, and the one or more devices on the second bus comprise a second plurality of cameras, and wherein all of the first and second pluralities of cameras are positioned to encircle an image area and to record images of the image area.